EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	419	717/106.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/03/30 14:42
L2	568	710/110.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/03/30 14:42
L3	1	710/110.ccls. and ("1 wire" or "one wire" or "one-wire" or "1-wire") and "half duplex"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/03/30 14:43
L4	8	710/110.ccls. and ("1 wire" or "one wire" or "one-wire" or "1-wire") and (master and slave)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/03/30 14:48
L5	58	("1 wire" or "one wire" or "one-wire" or "1-wire") and (master and slave) and "half duplex" and serial	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/03/30 14:50
L6	1	("1 wire" or "one wire" or "one-wire" or "1-wire") same (master and slave) same "half duplex" same serial	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/03/30 14:50
S1	236	717/100.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/03/30 13:45
S2	175	717/106.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2003/12/03 15:04
S3	128	717/107.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2003/12/03 15:04

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S4	229	717/108.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2003/12/03 16:38
S5	2	"20030074634"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2003/12/04 14:46
S6	60	(server-side or (server adj side)) adj objects	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2003/12/04 14:47
S7	7	(server-side or (server adj side)) adj objects same dynamic$4 and (web or page or content)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2003/12/04 14:48
S8	137	717/107.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/04/27 08:22
S9	260	717/108.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/04/27 07:32
S10	210	717/106.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/04/27 07:34
S11	2	"20030074634"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/04/27 07:34
S12	0	"20030074634".URPN.	USPAT	OR	OFF	2004/04/27 07:34
S13	279	717/100.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/04/27 08:12

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S14	13	717/107.ccls. and dynamic near3 (content or web or page)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/04/27 08:26
S15	13	717/108.ccls. and dynamic near3 (content or web or page)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/04/27 08:26
S16	40	("5748890" "5774670" "5812996" "5835724" "5897622" "5940075" "5953524" "5961601" "5986227" "5991802" "6014666" "6032207" "6076108" "6108717" "6115744" "6178461" "6185608" "6208480" "6212192" "6230160").pn.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/03/14 15:51
S17	40	("5748890" "5774670" "5812996" "5835724" "5897622" "5940075" "5953524" "5961601" "5983227" "5991802" "6014666" "6032207" "6076108" "6108717" "6115744" "6178461" "6185608" "6205480" "6212192" "6230160").pn.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/03/14 15:52
S18	0	("5748890" "5774670" "5812996" "5835724" "5897622" "5940075" "5953524" "5961601" "5983227" "5991802" "6014666" "6032207" "6076108" "6108717" "6115744" "6178461" "6185608" "6205480" "6212192" "6230160").pn. and (server-side or (server adj side)) adj objects same dynamic$4 and (web or page or content)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/03/14 15:56
S19	131	("5748890" "5774670" "5812996" "5835724" "5897622" "5940075" "5953524" "5961601" "5983227" "5991802" "6014666" "6032207" "6076108" "6108717" "6115744" "6178461" "6185608" "6205480" "6212192" "6230160").pn. creat$3 near5 (compil$3 near2 class)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/03/14 15:55
S20	69	("5748890" "5774670" "5812996" "5835724" "5897622" "5940075" "5953524" "5961601" "5983227" "5991802" "6014666" "6032207" "6076108" "6108717" "6115744" "6178461" "6185608" "6205480" "6212192" "6230160").pn. creat$3 near5 (compil$3 near2 class) and (generat$3 near3 source)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/03/14 15:56

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S21	72	("5748890" "5774670" "5812996" "5835724" "5897622" "5940075" "5953524" "5961601" "5983227" "5991802" "6014666" "6032207" "6076108" "6108717" "6115744" "6178461" "6185608" "6205480" "6212192" "6230160").pn. creat$3 near5 (compil$3 near2 class) and ((generat$3 or produce) near3 source)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/03/14 16:27
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S23	11	("5748890" "5774670" "5812996" "5835724" "5897622" "5940075" "5953524" "5961601" "5983227" "5991802" "6014666" "6032207" "6076108" "6108717" "6115744" "6178461" "6185608" "6205480" "6212192" "6230160").pn. and dynamic$4 near5 (web or page or content)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/03/14 15:56
S24	13	S23 andl6	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/03/14 15:57
S25	11	S23 and S21	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/03/14 15:57
S26	0	creat$3 near5 (compil$3 near2 class) and ((generat$3 or produce) near3 source) and dynamic$4 near5 (web or page or content) and "5517655".pn.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/03/14 16:28
S27	2	creat$3 near5 (compil$3 near2 class) and ((generat$3 or produce) near3 source) and dynamic$4 near5 (web or page or content) and ("20030025728" or "20030028565")	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/03/14 17:12

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S28	0	creat$3 near5 (compil$3 near2 class) and ((generat$3 or produce) near3 source) and dynamic$4 near5 (web or page or content) and ("6373841" "6397253" "6405241" "6460071" "6480894" "6557038" "6622168").pn.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/03/14 17:14
S29	0	creat$3 near5 (compil$3 near2 class) and ((generat$3 or produce) near3 source) and dynamic$4 near5 (web or page or content) and "20030028565"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/03/14 17:14
S30	2	"20030028565"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/03/14 17:17
S31	8	"20030009519" "2002008703" "20010054020"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/03/14 17:17
S32	6	"20030009519" "20020008703" "20010054020"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/03/14 17:19
S33	16	("6622168" "6557038" "6480894" "6460071" "6405241" "6397253" "6373841" "6247044").pn.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/03/14 17:20
S34	16	("5774670" "5835724" "5964601" "6076108" "6115744" "6178461" "6212192" "6230160").pn.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/03/14 17:21
S35	16	("5774670" "5835724" "5961601" "6076108" "6115744" "6178461" "6212192" "6230160").pn.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/03/14 17:21

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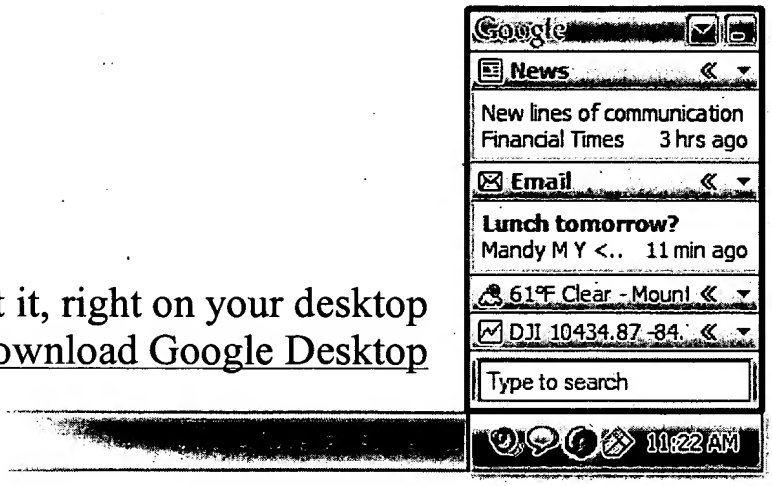

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1 BIST TPG for faults in system backplanes
Chen-Huan Chiang, Sandeep K. Gupta
November 1997 **Proceedings of the 1997 IEEE/ACM international conf Computer-aided design**
Publisher: IEEE Computer Society
Full text available: pdf (108.29 KB) Additional Information: full citation, abstr index terms
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A built-in self-test (BIST) methodology to test system backplanes by usi functionality in each of its constituent boards is presented. Since the con systems change frequently, at the system level, the proposed methodolo simple test schedule which can be easily changed whenever the system c changed. Since the boards used in such systems are designed for use in a systems, the proposed methodology defines the test objectives to be achi

Keywords: BIST circuit, BIST methodology, VME backplane, built-in s self-test, edge pin connections, programmable test architecture, simple te system backplanes, system configuration

2 Exploiting FPGA-features during the emulation of a fast reactive embedde
Karlheinz Weiß, Thorsten Steckstor, Gernot Koch, Wolfgang Rosenstiel
February 1999 **Proceedings of the 1999 ACM/SIGDA seventh internati on Field programmable gate arrays**
Publisher: ACM Press
Full text available: pdf(2.02 MB) Additional Information: full citation, refer index terms

3 Synthesis of signal processing structured datapaths for FPGAs supporting l
Baher Haroun, Behzad Sajjadi
February 1995 **Proceedings of the 1995 ACM third international sympo programmable gate arrays**
Publisher: ACM Press
Full text available: pdf (113.56 KB) Additional Information: full citation, abstr index terms

A novel approach is presented for transforming a given scheduled and bc processing algorithm for a multiplexer based datapath to a BUS/RAM ba datapath. A datapath model is introduced that allows maximum flexibilit bus transfers independent of operation scheduling. A novel integer linea (ILP) formulation that optimally selects and assigns data-transfers to bus scheduling the bus transfers to minimize a l ...

4 Illustrative risks to the public in the use of computer systems and related te
Peter G. Neumann
January 1996 **ACM SIGSOFT Software Engineering Notes**, Volume 21
Publisher: ACM Press
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5 An embedded DRAM architecture for large-scale spatial-lattice computatic
Norman Margolus
May 2000 **ACM SIGARCH Computer Architecture News , Proceeding annual international symposium on Computer architecture**

Volume 28 Issue 2
Publisher: ACM Press
Full text available: pdf (376.78 KB) Additional Information: full citation, abstr citings, index tern

Spatial-lattice computations with finite-range interactions are an importa parallelized computations. This class includes many simple and direct al physical simulation, virtual-reality simulation, agent-based modeling, lo and 3D image processing and rendering, and other volumetric data proce range of applicability of such algorithms is completely dependant upon t and processing speeds that are computationally fe ...

Keywords: PIM, cellular automata, lattice gas, virtual processor

6 Distributed systems - programming and management: On remote procedur
Patrícia Gomes Soares
November 1992 **Proceedings of the 1992 conference of the Centre for A on Collaborative research - Volume 2**
Publisher: IBM Press
Full text available: pdf(4.52 MB) Additional Information: full citation, abstr citings

The Remote Procedure Call (RPC) paradigm is reviewed. The concept is with the backbone structure of the mechanisms that support it. An overvi supporting these mechanisms is discussed. Extensions to the paradigm th proposed to enlarge its suitability, are studied. The main contributions of standard view and classification of RPC mechanisms according to differ and a snapshot of the paradigm in use today and of goals for t ...

7 Automatic synthesis of interfaces between incompatible protocols
Roberto Passerone, James A. Rowson, Alberto Sangiovanni-Vincentelli
May 1998 **Proceedings of the 35th annual conference on Design autom**
Publisher: ACM Press
Full text available: pdf (194.46 KB) Additional Information: full citation, abstr citings, index tern
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A t the system level, reusable Intellectual Property (or IP) blo cks can be abstractly as blocks that exchange messages. The concrete implementati blocks m ust exc hange the messages through complex signaling protoco ween IP that use different signaling protocols is a tedious and error pron propose using regular expression based protocol descriptions to sho w h message on to a signaling protocol. Given t w o protoc ...

Keywords: high-level synthesis, telecommunication

8 Practical experiences in interconnecting LANs via satellite

Nedo Celandroni, Erina Ferro, Francesco Potortì, Alessandro Bellini, Fran October 1995 **ACM SIGCOMM Computer Communication Review**, V **Publisher:** ACM Press

Full text available: pdf(1.12 MB) Additional Information: full citation, abstr terms

We present an experiment in interconnecting LANs via a satellite link ar individual components involved in the experiment. The project was deve phases: a) design and realisation of a satellite access scheme that suppor non real-time traffic with a signal fading countermeasure, called FODA/ interconnection of LANs where real-time and non real-time applications experiment was presented the first time in June 1994 as a demo in which

Keywords: TDMA fade countermeasure, satellite, satellite LAN interco videoconference

9 The design of RPM: an FPGA-based multiprocessor emulator

Koray Öner, Luiz A. Barroso, Sasan Iman, Jaeheon Jeong, Krishnan Rama Dubois

February 1995 **Proceedings of the 1995 ACM third international sympo programmable gate arrays**

Publisher: ACM Press

Full text available: pdf(54.01 KB) Additional Information: full citation, abstr citings, index tern

Recent advances in Field-Programmable Gate Arrays (FPGA) and progr interconnects have made it possible to build efficient hardware emulatio

addition, improvements in Computer-Aided Design (CAD) tools, mainly tools, greatly simplify the design of large circuits. The RPM (Rapid Prot Multiprocessors) Project leverages these two technological advances. Its a common hardware platform for th ...

Keywords: field-programmable gate arrays, logic emulation, message-p multicomputers, rapid prototyping, shared-memory multiprocessors

10 What is the cost of delay insensitivity?
Hiroshi Saito, Alex Kondratyev, Jordi Cortadella, Luciano Lavagno, Alexa
November 1999 **Proceedings of the 1999 IEEE/ACM international conf Computer-aided design**
Publisher: IEEE Press
Full text available: pdf (185.06 KB) Additional Information: full citation, abstr index terms

Deep submicron technology calls for new design techniques, in which w delays are accounted to have equal or nearly equal effect on circuit beha Asynchronous speed-independent (SI) circuits, whose behaviour is only delay variations, may be too optimistic. On the other hand, building circ insensitive (DI), for both gates and wires, is impractical. The paper prese for automated synthesis of globally DI and locally SI

11 A hardware-based performance monitor for the Intel iPSC/2 hypercube
Allen D. Malony, Daniel A. Reed
June 1990 **ACM SIGARCH Computer Architecture News , Proceeding international conference on Supercomputing ICS '90**, Volur
Publisher: ACM Press
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The complexity of parallel computer systems makes a priori performanc difficult and experimental performance analysis crucial. A complete cha software and hardware dynamics, needed to understand the performance performance parallel systems, requires execution time performance instr Although software recording of performance data suffices for low freque capture of detailed, high-frequency performance data ultimately r ...

12 A generic architecture for on-chip packet-switched interconnections
Pierre Guerrier, Alain Greiner
January 2000 **Proceedings of the conference on Design, automation and**
Publisher: ACM Press
Full text available: pdf (100.74 KB) Additional Information: full citation, refer
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13 A global synchronization network for a non-deterministic simulation archit
Marc Bumble, Lee Coraor
December 1999 **Proceedings of the 31st conference on Winter simulatio**
a bridge to the future - Volume 2
Publisher: ACM Press
Full text available: pdf (228.37 KB) Additional Information: full citation, refer
terms

14 High speed neural network chip for trigger purposes in high energy physics
W. Eppler, T. Fischer, H. Gemmeke, A. Menchikov
February 1998 **Proceedings of the conference on Design, automation an**
Publisher: IEEE Computer Society
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A novel neural chip SAND (Simple Applicable Neural Device) is descril usable for hardware triggers in particle physics. The chip is optimized fo rate (50 MHz, 16 bit data) at a very low cost basis. The performance of a chip is 200 MOPS due to four parallel 16 bit multipliers and 40 bit adder clock cycle. The chip is able to implement feedforward neural networks of 512 input neurons and three hidden layers. Kohonen feat ...

Keywords: VME board with neural network chip SAND, Hardware acc networks, High energy physics : trigger, on- and off-line analysis

15 A reconfigurable hardware approach to network simulation
Dimitrios Stiliadis, Anujan Varma
January 1997 **ACM Transactions on Modeling and Computer Simulati**
Volume 7 Issue 1
Publisher: ACM Press
Full text available: pdf (925.18 KB) Additional Information: full citation, refer index terms, revie

Keywords: ATM switch scheduling, field-programmable gate array, har

16 Evaluation of design alternatives for a multiprocessor microprocessor
Basem A. Nayfeh, Lance Hammond, Kunle Olukotun
May 1996 **ACM SIGARCH Computer Architecture News , Proceeding annual international symposium on Computer architecture**
Volume 24 Issue 2
Publisher: ACM Press
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In the future, advanced integrated circuit processing and packaging techr for several design options for multiprocessor microprocessors. In this pa three architectures: shared-primary cache, shared-secondary cache, and s We evaluate these three architectures using a complete system simulatio which models the CPU, memory hierarchy and I/O devices in sufficient run a commercial operating system. Within our simulation envir ...

17 SystemCSV - an extension of SystemC for mixed multi-level communicati interface-based system design
R. Siegmund, D. Müller
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L. Donnell Payne
March 1992 **Proceedings of the 1992 ACM/SIGAPP symposium on Ap technological challenges of the 1990's**
Publisher: ACM Press
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19 A high-performance host interface for ATM networks
C. Brendan S. Traw, Jonathan M. Smith
August 1991 **ACM SIGCOMM Computer Communication Review , Pr conference on Communications architecture & protocols** Volume 21 Issue 4
Publisher: ACM Press
Full text available: pdf (756.03 KB) Additional Information: full citation, refer index terms

20 Exploiting parallelism in pattern matching: an information retrieval applica
Victor Wing-Kit Mak, Kuo Chu Lee, Ophir Frieder
January 1991 **ACM Transactions on Information Systems (TOIS),** Vol
Publisher: ACM Press
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We propose a document-searching architecture based on high-speed hard matching to increase the throughput of an information retrieval system. V new parallel VLSI pattern-matching algorithm called the Data Parallel P (DPPM) algorithm, which serially broadcasts and compares the pattern t in parallel. The DPPM algorithm utilizes the high degree of integration c technology to attain very high-speed processing through parallelism. ...

Keywords: DPPM, pattern matcher

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